A low-power, high-linearity transconductor with high tolerance for process and temperature variations

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Abstract: A novel scheme for tunable CMOS transconductor robust against process and temperature variations is presented. The proposed configuration is a voltage controlled circuit based on a double NMOS transistor differential pairs connected in parallel, which has low power and high linearity. The process and temperature (PT) compensation is completed by two identical process and temperature compensation bias voltage generators (PTCBVG), which can guarantee the designed transconductor high tolerance for process and temperature variations. A complete CMOS transconductor with PTCBVG has been designed and simulated using 0.18μm technology. The effectiveness of PT compensation technique is proved. The simulation results of post-layout are commensurate with pre-layout. Post-layout simulation results show that when temperature changes from −40–85°C for different process corners (TT, SS, SF, FS, FF), the transconductance varies from 91.8–123.6μS, temperature coefficient is below 1090ppm/°C, the total harmonic distortion is from −78–72dB@1MHz for 0.2Vpp input signal, -3dB bandwidth changes from 2.5–5GHz, input referred noise varies from 78.1–124.8nV/sqrtHz@1MHz and DC power is from 1.5–3.2mW.

1. Introduction

The CMOS transconductor is a fundamental building block for analog signal processing circuits, such as amplifiers, multipliers, active filters and sinusoidal oscillators. Throughout the development of the state of the art, we can conclude that the performance indices of most concern about transconductor include high linearity, process and temperature (PT) compensation ability and low power.

The first and most important performance of the CMOS transconductor is its linearity. Up to now, all kinds of topologies of the CMOS transconductor have been presented for improving the linearity property. The main structure of the transconductor cell is the source-coupled differential pair, which has good CMRR, PSRR, low noise and excellent frequency performance. However, its large signal characteristics are nonlinear. Many advances in improving the linearity of CMOS transconductor circuits have been reported [1-25]. In [1], it proposes a transconductor with compensated source-coupled pair configuration. The circuit discussed have superior linearity and input voltage range compared with the conventional source-coupled differential pair. The proposed transconductor has a THD of approximately 0.1% covering one half the input voltage range, whereas the source-coupled pair exhibits a maximum error greater than 10% within this range. However, the bandwidth of the presented transconductor is only up to 6MHz by the simulation which is unsuitable for high frequency applications. In [2], it uses an approach to linearization by an electronically controlled current-mode cell. The linearity and input voltage range of the proposed circuits are significantly improved over those of the conventional source-coupled differential pair. The SPICE Simulated results show a linearity error less than 0.2% over ±4V differential input range for a power supply of ±5V. [5] presents a linear CMOS transconductor using triode transistors based on the scheme of flipped voltage follower current sensor. The transconductor cell biased in triode region presents simplicity and good programmability compared with its saturated-based counterpart. The proposed transconductor achieves a distortion of −91dB for a 1MHz, 1Vpp differential input voltage. [12-17] use the local feedback method to improve the linearity of the CMOS transconductor. The transconductor proposed by [12] is based in the creation of low impedance nodes using local feedback to drive a degeneration resistor. The presented transconductor doesn’t use current mirrors or nonlinearity cancellation method, which significantly improves the linearity and the robustness against mismatch. Simulation results show that the THD of the proposed transconductor can achieve −91dB at 10MHz with 2Vpp differential input-output signal. In [18-20], the source degeneration method is employed. [18] presents a programmable source degenerated telescopic cascade OTA improved by a very linear programmable degeneration resistor implemented with four quasi-floating-gates (QFS) transistors. The use of QFG transistors to implement the degenerated resistor has the advantage of providing programmability. What’s more, the harmonic distortion factor for the resistor used here is better than the case of using a triode transistor as a resistance. The simulation results obtained show a THD of −61dB at 10MHz for a 1Vpp output voltage. [21-25] discuss the non-linearity cancellation method. Transconductors with differential pairs based on nonlinearity cancellation have demonstrated good performances at high frequencies, but the process and temperature variations will greatly reduce the effectiveness of nonlinearity cancellation method. [22] presents a nonlinearity cancellation technique low sensitive to process-temperature-bias current variations. The proposed OTA is realized by using complementary triple differential pairs. Experimental results of the proposed circuit show that the transconductor achieves IM3=−70dB for a two-tone 1.3Vpp input signal for frequencies up to 70MHz with 9.5mW of power consumption.
Recently, for broadening the application of the CMOS transconductor, how to improve the tolerance for process and temperature variations has received more and more attention. [29] presents a fully on-chip process and temperature (PT)-invariant transconductor circuit that doesn’t need any accurate quantity or trimming/calibration. The proposed transconductor employs a PTAT voltage generator, a process tracking circuit and a beta multiplier-based bias circuit. Measurement results show that the transconductance varies only by ±3.4% across 18 fabricated chips and over temperatures ranging from 25°C to 100°C. [32] presents a tunable body biasing voltage generated by auxiliary bandgap, LDO and body voltage control circuit to calibrate the transconductance induced by temperature. The accuracy of the transconductor is nearly ±0.092%. However, the simulation results of [32] can’t support its conclusion, because the influence of process variations and device mismatch on the transconductance variation is competitive to the temperature variation. More simulation work especially the montecarlo simulations need to be performed to verify the effectiveness of the theoretical analysis in [32].

Also, there are many reports about the low power design of the CMOS transconductor. The most popular low power topology of the transconductor is the pseudo differential pair [13, 26-27]. However, the pseudo differential structure usually has poor rejection to common-mode signals, which therefore can originate a large amount of distortion. The common-mode feedback circuit can overcome this drawback, but it increases both noise and power consumption. Although the technique for common-mode signals cancellation has been used, the CMRR performance of the pseudo-differential transconductor is inferior to the classical fully-differential one particularly at low frequency [26].

According to the discussion above, this paper employs a double differential pairs as the topology of the CMOS transconductor and the process and temperature compensation bias voltage generator (PTCBVG) to complete the process and temperature compensation function of the transconductor. The basic principle of the circuit is described in section II. The design scheme for process and temperature compensation is discussed in section III. Simulation results are presented in section IV. Conclusions are drawn in section V.

2. The basic principle of the transconductor

Fig. 1 provides the basic circuit diagram of the proposed CMOS transconductor core, $V_{ad}$ and $V_{an}$ are the two differential input voltages, and $I_{ad}$ and $I_{an}$ are the two differential output currents. The topology of the proposed transconductor in Fig. 1 is based on a double NMOS transistor differential pairs connected in parallel, which is similar to the topology in [28]. As is shown in Fig. 1, the double NMOS transistor differential pairs consist of two NMOS transistor differential pairs of $M_{N1T}$ and $M_{N2T}$, and $M_{N3T}$ and $M_{N4T}$, which operate in their saturation regions. The current of $I_1$, $I_2$, $I_3$ and $I_4$ respectively represents the drain current of the NMOS transistor $M_{N1T}$, $M_{N2T}$, $M_{N3T}$ and $M_{N4T}$. The drain current of PMOS transistor $M_{P1T}$ equals $I_{1}+I_{2}$, and the drain current of PMOS transistor $M_{P2T}$ equals $I_{3}+I_{4}$. The current mirrors of PMOS transistor $M_{P1T}$, $M_{P2T}$, $M_{P3T}$ and $M_{P4T}$, NMOS transistor $M_{N1T}$ and $M_{N1T}$, and NMOS transistor $M_{N3T}$ and $M_{N3T}$ act as active loads, which make $I_{d1}=I_{1}+I_{2}$ and $I_{d2}=I_{3}+I_{4}$.

Now let us calculate the linearity property of the double differential pairs of the transconductor presented in Fig. 1. We assume that all the MOS transistors of the transconductor circuit work in saturation region. Without considering the second-order effects of the MOS transistors, the $I-V$ characteristics of the proposed transconductor can be expressed as

\[
I_1 = K_n (V_{ad} - V_A - V_{tn})^2 \quad (1a)
\]

\[
I_2 = K_n (V_{an} - V_A - V_{tn})^2 \quad (1b)
\]

\[
I_3 = K_n [(V_{ad} - V_{T1}) - V_B - V_{tn}]^2 \quad (1c)
\]

\[
I_4 = K_n [(V_{an} - V_{T1}) - V_B - V_{tn}]^2 \quad (1d)
\]

\[
I_{s1} = 2K_n (V_{T2} - V_{tn})^2 \quad (1e)
\]

\[
I_{s2} = 2K_n (V_{T3} - V_{tn})^2 \quad (1f)
\]

where $I_1$, $I_2$, $I_3$ and $I_4$ are the drain currents of the NMOS transistor $M_{N1T}$, $M_{N2T}$, $M_{N3T}$ and $M_{N4T}$ respectively; $I_{s1}$ and $I_{s2}$ are the drain currents of the NMOS transistor $M_{N5T}$ and $M_{N6T}$; $V_{ad}$ and $V_{an}$ are the two differential input voltages; $V_A$ and $V_B$ are the terminal voltages of the node A and B; $V_{T1}$, $V_{T2}$ and $V_{T3}$ are the external DC voltages; $V_{thn}$ is the threshold voltage of the NMOS transistor; $K_n=(1/2)\mu C_{ox}(W/L)$, where $\mu$ represents the electron mobility, $C_{ox}$ is the gate oxide capacitance per unit area, and $W$ and $L$ are the width and length of the channel respectively. In (1a) to (1d), we assume that the double NMOS transistor differential pairs ($M_{N1T}$-$M_{N1T}$) have the same aspect ratio ($W/L$). For ease of analysis, as can be seen in (1e) and (1f) we also assume that the NMOS transistor $M_{N5T}$ and $M_{N6T}$ have twice the aspect ratio of the double NMOS transistor differential pairs.

We write the input voltages of the transconductor as

\[
V_{ad} = V_1 + V_{id} \quad (2a)
\]

\[
V_{an} = V_1 - V_{id} \quad (2b)
\]

where $V_1$ represents the common-mode part of the input voltage and $V_{id}$ is the differential-mode part of the input voltage.

Using KCL for node A and B, we can get

\[
I_{s1} = I_1 + I_2 \quad (3a)
\]

\[
I_{s2} = I_3 + I_4 \quad (3b)
\]

Substituting (1a)-(1f) and (2a)-(2b) in to (3a) and (3b), and calculating the difference between $I_{s1}$ and $I_{s2}$, we can get

\[
V_A = V_1 - V_{T2} \quad (4a)
\]

\[
V_B = V_1 - V_{T1} - V_{T3} \quad (4b)
\]
Using (1a)-(1b), (2a)-(2b) and (4a), we can obtain the difference between $I_1$ and $I_2$
\[ I_1 - I_2 = 4K_a V_{sd} (V_{T2} - V_{th}) \] (5)

Using (1c)-(1d), (2a)-(2b) and (4b), we can also obtain the difference between $I_3$ and $I_4$
\[ I_3 - I_4 = 4K_a V_{sd} [V_{T3} - V_{th}] \] (6)

Now based on (5) and (6), the output currents of the transconductor become:
\[ I_{sd} = I_1 + I_3 - I_2 - I_4 = 4K_a V_{sd} (V_{T2} + V_{T3} - 2V_{th}) \] (7a)
\[ I_{sd} = I_2 + I_4 - I_1 - I_3 = 4K_a V_{sd} (V_{T2} + V_{T3} - 2V_{th}) \] (7b)

So the transconductance of the proposed transconductor can be expressed as
\[ G_m = 4K_a (V_{T2} + V_{T3} - 2V_{th}) \] (8)

Observing (7) and (8), we can find that the linearity property of the double differential pairs of the proposed transconductor is expressed as an ideal linear mathematical model, and the transconductance is a constant which is proportional to the external DC voltages of $V_{T2}$ and $V_{T3}$.

3. The design scheme for process and temperature compensation

According to [33], we can know that most process parameters vary with temperature, if a circuit is temperature-independent, then it is usually process-independent as well. So if the derivative of $G_m$ in (8) with respect to the absolute temperature $T$, $\partial G_m / \partial T$, is equal to zero, the gain of the transconductor will be independent of both process and temperature. Based on this premise, we introduce a novel technique to complete the process and temperature compensation of the transconductor.

3.1. The design of process and temperature compensation bias voltage generator

The design scheme for process and temperature compensation of the proposed transconductor is illustrated in Fig. 2, which provides the circuit diagram of the devised process and temperature compensation bias voltage generator (PTCBVG). The presented PTCBVG is composed of a supply-independent biasing circuit, a PMOS core and an output part. All the MOS transistors of the PTCBVG work in saturation region except the PMOS transistors of $M_{P4V}$, $M_{P5V}$ and $M_{P6V}$ which are in subthreshold region. What’s more, $k$ is the aspect ratio of $M_{P4V}$ and $M_{P5V}$ to $M_{P6V}$, $R_1$ and $R_2$ are two voltage controlled resistors and $V_T$ is the output voltage of the PTCBVG circuit.

First, we assume that the PMOS transistors of $M_{P1V}$, $M_{P2V}$ and $M_{P3V}$ have the same size, and so do the NMOS transistors of $M_{N1V}$ and $M_{N2V}$. Next, tuning the DC bias point of the PTCBVG makes $V_C = V_D$. Then, we can acquire the same current flow behaviors of $M_{P1V}$, $M_{P2V}$ and $M_{P3V}$:
\[ I_{sdP1V} = I_{sdP2V} = I_{sdP3V} = I_5 \]
where $I_{sdP1V}$, $I_{sdP2V}$ and $I_{sdP3V}$ respectively represents the source-drain current of $M_{P1V}$, $M_{P2V}$ and $M_{P3V}$.

In order to illustrate the working principle of the PTCBVG, we introduce a mathematical model of the source-drain current of the PMOS transistor (BSIM3V3 model) in subthreshold region,
\[ I_{sd} = I_{so} \left[ 1 - \exp \left(-\frac{V_{sd}}{V_{th}}\right) \right] \exp \left(\frac{V_{sd} - V_{th}}{V_{th}}\right) \] (9)
\[ I_{so} = \mu_p \frac{W_{eff}}{L_{eff}} \sqrt{\frac{qC \cdot N_C \cdot V_i^2}{4\phi_k}} \] (10)
where \( I_{ds} \) is a specific current; \( V_{sd} \) is the source-drain voltage of the PMOS transistor; \( n \) is the subthreshold swing factor, the typical value of which is 2; \( \psi \) is the thermal voltage, \( \psi = k_B T q \), where \( k_B \) is the Boltzmann constant and \( k_B = 1.4 \times 10^{-23} \text{J/K} \), \( T \) is the absolute temperature, and \( q \) is the electron charge; \( V_{sg} \) is the source-gate voltage of the PMOS transistor; \( V_{th} \) is the threshold voltage of the PMOS transistor; \( V_{ON} \) is the offset voltage of the BSIM3V3 model in the subthreshold region, the recommended range for which is between \(-0.06\text{V}\) and \(-0.12\text{V}\). The default value of \( V_{OFF} \) is \(-0.08\text{V}\), which is an offset voltage of the BSIM3V3 model in the overdrive region.

According to (10), (12) can be changed as

\[
 V_{sd} - V_{ap} - V_{OFF} = V_{sg} = n \psi \ln \left( \frac{I_s}{I_{sg}} \right)
\]  

(11)

where \( V_{sd} \) represents the overdrive voltage of the PMOS transistor working in the subthreshold region.

So the source-gate voltage difference of PMOS transistor \( M_{PV5} \) and \( M_{PV6} \), \( V_{ap} - V_{OFF} \), can be expressed as

\[
 V_{ap} - V_{OFF} = n \psi \ln \left( \frac{I_s}{I_{ap}} \right) - n \psi \ln \left( \frac{I_s}{I_{sg}} \right)
\]  

(12)

where \( I_s \) is the source-drain current of the PMOS transistor \( M_{PV5} \) and \( M_{PV6} \); \( I_{ap} \) and \( I_{sg} \) represent the specific currents of the PMOS transistor \( M_{PV5} \) and \( M_{PV6} \), respectively.

According to (10), (12) can be changed as

\[
 V_{ap} - V_{OFF} = n \psi \ln k
\]  

(13)

where \( k \) is the aspect ratio of \( M_{PV5} \) to \( M_{PV6} \).

\[ V_{ap} - V_{OFF} \] also means the voltage drop across the resistor \( R \), so the current flowing through \( R \) is equal to \( n \psi \ln k \), which also equals the source-drain current of the PMOS transistor \( M_{PV4} \) and \( M_{PV6} \). Then we can get the expression of \( V_{T} \) as

\[
 V_{T} = V_{ap} - V_{OFF} + n \frac{R}{R_1} \psi \ln k
\]  

(14)

where \( V_{ap} \) is the source-gate voltage of the PMOS transistor \( M_{PV4} \).

### 3.2. The complete schematic of the proposed transconductor

Fig. 3 shows the complete transconductor circuit, which contains three major parts: the CMOS transconductor core depicted in Fig. 1, and the two identical process and temperature compensation bias voltage generators (PTCBVG) depicted in Fig. 2 which are used to provide the external DC voltages of \( V_{T1} \) and \( V_{T2} \) for the CMOS transconductor core. Importantly, the resistors \( R_1 \) and \( R_2 \) in Fig. 2 are substituted by the NMOS transistor \( M_{R1} \) and \( M_{R2} \), and \( M_{R3} \) and \( M_{R4} \) in Fig. 3, which are controlled by the DC voltage \( V_{R1}, V_{R2}, V_{R3} \) and \( V_{R4} \), respectively.

According to (14), we can get the expressions of \( V_{T2} \) and \( V_{T3} \)

\[
 V_{T2} = V_{ap} - V_{OFF} + n \frac{R}{R_1} \psi \ln k
\]  

(15a)

\[
 V_{T3} = V_{ap} - V_{OFF} + n \frac{R}{R_3} \psi \ln k
\]  

(15b)

where \( V_{ap} \) and \( V_{ap} \) represent the source-gate voltages of \( M_{PV4} \) and \( M_{PV6} \) respectively.

Assuming that \( V_{ap} = V_{ap} \), then substituting (15a) and (15b) into (8), we can get

\[
 G_m = 4K_n \left( V_{ap} - V_{ap} + n \frac{R}{R_1} \psi \ln k + n \frac{R}{R_3} \psi \ln k \right)
\]  

(16)

The derivative of \( G_m \) in (16) with respect to the absolute temperature \( T \) can be expressed as

\[
 \frac{\partial G_m}{\partial T} = 2C_m W L \frac{\partial \mu_p}{\partial T} \left( V_{ap} + V_{ap} + n \frac{R}{R_1} \psi \ln k + n \frac{R}{R_3} \psi \ln k \right)
\]  

(17)

By the way, \( \mu_p \) in (10) and \( \mu_n \) in (17) can be expressed as

\[
 \mu_p = \mu_{p0} \left( \frac{T_{SOM}}{T} \right)^{\nu_p}
\]  

(18a)

\[
 \mu_n = \mu_{n0} \left( \frac{T_{SOM}}{T} \right)^{\nu_n}
\]  

(18b)
where $\mu_{op}$ and $\mu_{on}$ are the hole and electron mobility temperature exponent parameters at the temperature of $T_{\text{NOM}}$; $T_{\text{NOM}}$ is the parameter measurement temperature, the default value of which is 27°C; $\mu_{TE}$ is the mobility temperature exponent parameter, the default value of which is −1.5.

Now let us take the derivative of $\mu_n$ in (18b) with respect to the absolute temperature $T$, we can get

$$\frac{\partial \mu_n}{\partial T} = \frac{-\mu_{TE} \mu_n T_{\text{NOM}}}{T V_{T}}$$

(19)

According to (10), (11) and (18a), we can get the derivative of the overdrive voltage of the PMOS transistor operating in subthreshold region with respect to the absolute temperature $T$

$$\frac{\partial V_{\text{ovp}}}{\partial T} = \frac{V_{\text{ovp}} - n \mu_{op}}{T} \left(2 - |\mu_{op}|\right)$$

(20)

Now we substitute (19) and (20) into (17), then (17) becomes (21).

Equation (21) gives the temperature coefficient of the transconductor at a given temperature $T$, which is dependent on the values of $V_{\text{ovp}}$ and $V_{\text{ovp}}$, the ratio of $R_2$ to $R_1$ and the ratio of $R_4$ to $R_3$. This means that tuning the ratio of $R_2$ to $R_1$ and the ratio of $R_4$ to $R_3$ can compensate the process and temperature variations of the transconductor.

We define the voltage parameters of $V_{Rs}$, $V_{R2}$, $V_{R3}$, $V_{R4}$ and $V_{T1}$ based on the principle of the flowchart in Fig. 4.

4. Simulation results

The proposed CMOS transconductor is designed in 0.18μm process. The aspect ratios of the MOS transistors in the complete transconductor circuit are listed in Table I. For reducing the transconductance deviation induced by process variations and device mismatch, we choose $V_{Rs}$ = 1.8V. $V_{R2}$ and $V_{R4}$ are generated by the reference voltage divider of Fig.5. Fig. 6 is the layout of the presented transconductor. The transconductor occupies an area of 49×24μm$^2$. High performance simulations using the Spectre Circuit Simulator have been performed to verify the theoretical analysis.

$$\frac{\partial G_m}{\partial T} = 2\mu_n C_m \frac{W}{L} \frac{T_{\text{NOM}}}{T} \left[\left(\mu_{op} - 1\right) \left(V_{\text{ovp}} - q \mu_{op} \ln n \mu_{op} + n \frac{R_4 K_a}{R_2 q} \ln k - n \frac{K_a}{R_2 q} \ln k\right) - 2\left(\mu_{op} \left|n \frac{K_a}{q}\right|\right)\right]$$

(21)

4.1. Verification of the compensation technique of the proposed transconductor

For illustrating the improvement of the proposed transconductor with PT compensation technique, we perform montecarlo simulations to compare the proposed transconductor without (Fig. 1) and with the compensation technique (Fig. 3). The number of samples is 50. Figs. 7a-b show the transconductance variation over temperature (−40-85°C) with process variations and device mismatch. The min ($G_{m,min}$) and max ($G_{m,max}$) statistics of Fig. 7 drawn in Fig. 8 indicate that the transconductance variation ranges of the proposed transconductor without and with PT compensation are equal to 96-140μS and 96 -132μS, respectively. Fig. 9 shows that the DC power of the transistor without and with PT compensation technique equals 1.6-2.8mW and 1.6-2.9mW. Fig. 10 presents the relative deviation error of proposed transconductor ($G_{m,max}/G_{m,min}$) without and with PT compensation technique: 0.8-7.9%, 0.7-5.6%. What’s more, we can find that 98% relative deviation error of the proposed transconductor with PT compensation technique is below 5%. However, 26% relative deviation error of the proposed transconductor without PT compensation technique is above 5%. The min and max statistics shown in Fig. 11 present the temperature coefficient of the proposed transconductor without and with PT compensation technique: ≤1400ppm/°C, ≤900ppm/°C.

<table>
<thead>
<tr>
<th>MOS transistors</th>
<th>Dimension (W/L)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MN1T-MN4T, MN7T-MN18T, MN1V-MN4V, MR1-MR4, MN1D-MN5D</td>
<td>0.5/0.18μm</td>
</tr>
<tr>
<td>MN5T-MN6T</td>
<td>1/0.18μm</td>
</tr>
<tr>
<td>MP1T-MP6T, MP1V-MP3V, MP6V, MP7V-MP9V, MP12V, MP1D-MP3D</td>
<td>2/0.18μm</td>
</tr>
<tr>
<td>MP5D</td>
<td>3/0.18μm</td>
</tr>
<tr>
<td>MP4V-MP5V, MP10V-MP11V</td>
<td>4/0.18μm</td>
</tr>
<tr>
<td>MP4D</td>
<td>6/0.18μm</td>
</tr>
</tbody>
</table>
First, confine the values of $V_{R1}$, $V_{R2}$, $V_{R3}$, $V_{R4}$, and $V_{T1}$ to a very range that guarantee the proposed transconductor shown in Fig. 3 is biased at DC operating point when the circuit works at each combination of the five process corners ($TT$, $SS$, $SF$, $FS$, $FF$) and the three temperatures ($-40^\circ C$, $27^\circ C$ and $85^\circ C$).

Then, choose the value of $V_{R2}$ to make the PMOS transistors of $M_{PV1}$, $M_{PV2}$ and $M_{PV3}$ in Fig. 3 work in the subthreshold region and the PMOS transistors of $M_{PV1}$, $M_{PV2}$ and $M_{PV3}$ in Fig. 3 have the same current flow behaviors, and let $V_{R3}$ take the same value with $V_{R1}$.

Finally, choose the value of $V_{R2}$ and $V_{R3}$ to make the proposed transconductor have the lowest temperature coefficient.

**Fig. 4.** The flowchart of how to choose the voltage parameters of $V_{R1}$, $V_{R2}$, $V_{R3}$, $V_{R4}$, and $V_{T1}$

**Fig. 5.** Circuit diagram of the voltage reference divider

**Fig. 6.** Layout of the complete transconductor

**Fig. 7.** Transconductance deviation over temperature (a) without and (b) with PT compensation technique

**Fig. 8.** The min and max transconductance statistics of the proposed transconductor over temperature
Table II summarizes the performance comparison between the proposed transconductor without and with compensation technique. It can be seen that the transconductor with PT compensation technique has higher tolerance for process and temperature variations than the one without PT compensation technique but hardly consumes more DC power.

<table>
<thead>
<tr>
<th>Performance Comparison</th>
<th>Without Compensation Technique</th>
<th>With Compensation Technique</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transconductance variation over temperature with process variations and device mismatch</td>
<td>96-140μS</td>
<td>96-132μS</td>
</tr>
<tr>
<td>The relative deviation error of the proposed transconductor over temperature</td>
<td>0.8-7.9%</td>
<td>0.7-5.6%</td>
</tr>
<tr>
<td>Temperature coefficient of the proposed transconductor</td>
<td>≤1400ppm/°C</td>
<td>≤900ppm/°C</td>
</tr>
<tr>
<td>Power dissipation over temperature</td>
<td>1.6-2.8mW</td>
<td>1.6-2.9mW</td>
</tr>
</tbody>
</table>

Table II summarizes the performance comparison between the proposed transconductor without and with compensation technique. It can be seen that the transconductor with PT compensation technique has higher tolerance for process and temperature variations than the one without PT compensation technique but hardly consumes more DC power.

4.2. Performance comparison of pre-layout and post-layout simulation

Fig. 12 provides the transconductance variation of the proposed transconductor over temperature for different process corners: 92.3-123.3μS (pre-layout), 91.8-123.6μS (post-layout). Fig. 13 presents the temperature coefficient of the proposed transconductor: ≤1030ppm/°C (pre-layout), ≤1090ppm/°C (post-layout). Fig. 14 shows the DC power dissipation of the proposed transconductor: 1.5-3.3mW (pre-layout), 1.5-3.2mW (post-layout). According to Fig. 15, we can find that the THD of the proposed transconductor is below -40dB at 1MHz over one sixth the input voltage range. The THD of pre-layout simulation is -82-72dB at 1MHz for 0.2Vpp input voltage and the THD of post-layout simulation is -78-72dB at 1MHz for 0.2Vpp input voltage. Fig. 16 presents the bandwidth of the transconductor over temperature for different corners: the pre-layout simulation result is from 3.5-7.5GHz, the post-layout simulation is from 2.5-5GHz. Based on Fig. 17, we can get the noise performance of the proposed transconductor: the input referred noise of the pre-layout simulation is from 75.4-125.4nV/sqrtHz at 1MHz, the input referred noise of the post-layout simulation is from 78.1-124.8nV/sqrtHz at 1MHz. Table III summarizes the performance comparison between pre-layout and post-layout simulation results, from which we can conclude the post-layout simulation results are quite close to the pre-layout.
**Fig. 12.** The transconductance variation of the proposed transconductor over temperature for different process corners

**Fig. 13.** Temperature coefficient of the proposed transconductor over temperature for different process corners

**Fig. 14.** Power dissipation of the proposed transconductor over temperature for different process corners

**Fig. 15.** Total harmonic distortion of the proposed transconductor at 1MHz over differential input voltage

**Fig. 16.** The normalized transconductance of the proposed transconductor
Table IV compares the performance of the proposed transconductor based on double differential pairs with other types of topology, such as the topologies of source-coupled differential pair [6], cross-coupled differential pair [11], local feedback [12, 17], source degeneration [20], nonlinearity cancellation method [22], the one with PT compensation technique [29], and the pseudo differential pair [13]. The comparison results demonstrate that the proposed transconductor has the lowest temperature coefficient and the second widest bandwidth among the reported works with comparatively low power dissipation and high linearity property. However, the linear input voltage range of the proposed transconductor is narrow, which will be solve in our future work.

5. Conclusions
This paper proposes a novel CMOS transconductor based on a double NMOS transistor differential pairs with process and temperature (PT) compensation technique. The simulation results show that the proposed transconductor has high linearity and strong tolerance for process and temperature variations with relative low power.

6. Acknowledgments
This research was supported by Major State Basic Research Development Programme of China (2018YFE020091).
### Table IV Performance comparison with some reported transconductors

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<tr>
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<td>Source-coupled differential pair</td>
<td>Cross-coupled differential pair</td>
<td>Local feedback</td>
<td>Local feedback</td>
<td>Source degeneration</td>
<td>Non linearity cancellation</td>
<td>Process and temperature compensation</td>
<td>Pseudo differential pair</td>
<td>Double differential pair</td>
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<td>Technology (μm)</td>
<td>0.5</td>
<td>0.18</td>
<td>0.5</td>
<td>0.13</td>
<td>0.18</td>
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<td>Supply voltage (V)</td>
<td>±1.65</td>
<td>1.8</td>
<td>3.3</td>
<td>1.2</td>
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<td>Gm (μS)</td>
<td>&lt;55</td>
<td>1.8-31.13</td>
<td>/</td>
<td>12500</td>
<td>/</td>
<td>1200</td>
<td>/</td>
<td>50-200</td>
<td>91.8-123.6</td>
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<td>Temperature coefficient (ppm/°C)</td>
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<td>/</td>
<td>/</td>
<td>/</td>
<td>/</td>
<td>14000</td>
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<tr>
<td>Linear input voltage range (V)</td>
<td>0.5</td>
<td>0.4</td>
<td>2</td>
<td>0.33</td>
<td>0.2</td>
<td>1.3</td>
<td>/</td>
<td>1</td>
<td>0.2</td>
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<tr>
<td>IM3 (dB)/THD (dB)</td>
<td>-82 @1MHz, 0.5Vpp</td>
<td>/</td>
<td>-48 @1MHz, 0.4Vpp</td>
<td>-81dB @10MHz, 2Vpp</td>
<td>/</td>
<td>-91 @1MHz, 0.2Vpp</td>
<td>/</td>
<td>-72 @100KHz, 0.13Vpp</td>
<td>/</td>
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<tr>
<td>-3dB bandwidth (MHz)</td>
<td>/</td>
<td>185-1610</td>
<td>/</td>
<td>20000</td>
<td>/</td>
<td>/</td>
<td>/</td>
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<td>40</td>
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<td>Input referred noise (nV/sqrtHz)</td>
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<td>1.75</td>
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<td>7</td>
<td>/</td>
<td>61@5MHz</td>
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<td>Power consumption (mW)</td>
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<td>9.5</td>
<td>0.136</td>
<td>1.25</td>
<td>1.5-3.2</td>
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</table>

7. References

with 90dB SFDR and low sensitivity to mismatch'. IEEE ISCAS 2006, Island of Kos, Greece, 2006, pp. 69-72


